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P2.092 FPGA-based interlock system for the chopper of the Linear IFMIF prototype accelerator injector

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The Linear IFMIF (International Fusion Materials Irradiation Facility) Prototype Accelerator (LIPAc) injector consists of a 140 mA proton/deuteron source, its associated low energy beam transport line (LEBT) as well as ancillaries such as water cooling skid, vacuum groups, High Voltage Power Supplies (HVPS), etc . A specific element, the beam “Chopper”, was included in the LEBT to generate short (~ 100μs) and sharp edged beam pulses (~10μs) and allow the use of interceptive diagnostics in the high energy part of the LIPAc during commissioning phases of the RFQ (5MeV) and the SRF Linac (9MeV). The chopper was designed to operate in pulsed mode with very sharp rise and fall times, meaning the chopper will be used to “cut” the long rise time of the source as well as the fall time of the beam pulse.
The chopper thermal screen has not been designed to withstand very high beam power (i.e. beam length and duty cycle need to be monitored); in addition, the chopper HVPS needs to be monitored in real time to detect a possible trip and extract the beam before downstream devices are damaged. For these applications, standard PLC based interlocks are too slow and faster solutions are envisaged.
The proposed solution for the required interlock system is based on COTS technology based on XILINX FPGAs using RIO (Reconfigurable Input/Output) technology from National Instruments (CompactRIO platform), that provides reconfigurable FPGA-based embedded system for control and data acquisition applications. The paper describes the implementation of the interlock system, the response times of the proposed architecture and the performance of the system. Also, the CompactRIO contains a microcontroller running a real-time Linux operating system and uses LabVIEW Channel Access Server and Client to interface with EPICS in order to monitor and control the interlock system.

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